REMARKS

Claims 1-16 and 25 to 40 remain in this application. Currently, claims 1, 9, 29 and 35 are the sole remaining independent claims in connection with the present application.

Final Rejection Improper

The Examiner alleges that the present rejection has been made final since Applicant's previous amendments necessitated each of the various new grounds of rejection in connection with the present application. However, with regard to the Examiner's rejection of claims 6 and 14 under 35 U.S.C. 112, second paragraph for example, there is no amendment to these claims which necessitated to the Examiner's rejection. The Examiner could of easily made the same rejection in the first initial Office Action issued by the Examiner. Accordingly, as Applicant's amendment did not necessitate this new grounds of rejection made by the Examiner, **the Examiner's rejection should not of been made final.** Accordingly, withdrawal of finality of the Examiner's rejection and **entry of all of Applicant's amendments as a matter of right** is respectfully requested in connection with the present application.

Objection to the Drawings

The Examiner has objected to the drawings under 37 CFR 1.83(a). The Examiner has alleged that the drawings do not show every feature of the invention as specified in the claims. Applicant respectfully traverses this objection for the following reasons.

The Examiner alleges that the first bond pad or first electrical termination means (as recited in claims 1 and 9 respectively) and the second bond pad or second electrical termination means (as recited in claims 6 and 14 respectively) of the at least one pair of bond pads or one pair of electrical termination means located in the internal portion of the semiconductor die, must be shown or the features are canceled from the claims.

Applicant respectfully submits that claims 6 and 14 have been corrected to clarify that the second bond pad or second electrical termination means is located in a non-internal portion of the semiconductor die. Thus, Figures 1-4 of the present application show various embodiments of the present application, each including the second bond pad or second electrical termination means on a non-internal portion of the semiconductor die (bond pad 34a in Fig. 2, 52a in Fig. 3, and 74a in Fig. 4 for example); and a first bond pad or first electrical termination means located in an internal portion of the semiconductor die (bond pad 34b in Fig. 2, 52b in Fig. 3, and 74a in Fig. 4 for example). As such, the claims and drawings are consistent and no changes need to be made to the drawings. Thus, such an objection to the drawings should be withdrawn.

Furthermore, the Examiner alleges that "a package" as recited in claims 1, 9, 29, and 35 is not shown in the drawings. Again, Applicant traverses this objection as the leads of a package are shown in each of Figures 1-4, as represented by at least elements 14 in Fig. 1, 40 in Fig. 2, 60 in Fig. 3, and 80 in Fig. 4 for example. Thus, again, Applicant respectfully requests withdrawal of the Examiner's objection.

Claim Objections

The Examiner further objects to claims 36-39 for minor informalities, alleging that the claims lack antecedent basis. In response thereto, Applicant notes that claims 36-40 were added at the same time as new independent claim 35, and were supposed to be dependent on new independent claim 35. By the present Amendment, Applicant has corrected this typographical error such that each of claims 36-40 now depend from independent claim 35 and do contain appropriate antecedent basis and are not duplicative of any other claims. Accordingly, withdrawal of the Examiner's rejection is respectfully requested.

Claim Rejections Under 35 U.S.C. 112

The Examiner has rejected claims 1-16, 25-28, and 29-40 under 35 U.S.C. 112, first paragraph. This rejection is respectfully traversed.

It appears that with regard to each of claims 1, 9, 29, and 35, the Examiner objects to Applicant's claiming of a connection to an electrical package. As previously stated, Applicant's drawings provide support for connection to at least a lead wire of a package. Further, Applicant's detailed description provides even more support for such a limitation. For example, paragraph 0009 of the present application mentions that a semiconductor device may be mounted in any suitable package such as QFPs and PBGAs (identified as Quad Flat Packs and Pin Ball Gate Arrays, respectively). Thus, for at least the aforementioned reasons, withdrawal of the Examiner's rejection under 35 U.S.C. 112, first paragraph is respectively requested.

Rejection Under 35 U.S.C. 112, Second Paragraph

The Examiner has rejected claims 1-6, 25-28, and 29-40 under 35 U.S.C. 112, second paragraph. This rejection is respectfully traversed.

In response to the Examiner's rejections, Applicant has amended claims 6 and 14 to clarify that the second bond pad is located at a non-internal portion of the semiconductor die, as suggested by the Examiner. Thus, withdrawal of the Examiner's rejection of claims 6 and 14 is respectfully requested.

Further, the Examiner rejects claims 1, 9, 29, and 35, alleging that the recitation of "for electrically connecting to a package" is unclear. Applicant respectfully traverses this rejection. However, as the connection to a package is clearly disclosed and shown in the figures, Applicant respectfully submits that the aforementioned claim language is clear, especially when read in light of the present specification. In addition, new claims 29 and 35 have either been further

amended, to clarify that the electrical connection is to leads of the package, wherein the leads are spaced from periphery of the semiconductor die. Accordingly, for at least such reasons, Applicant respectfully requests withdrawal of the Examiner's rejection of claims 1, 9, 29, and 35, and all claims dependent thereon.

Prior Art Rejections

The Examiner has rejected claims 29-31 and 33-35 under 35 U.S.C. 102(e) as being anticipated by Schoenfeld. This rejection is respectfully traversed.

Schoenfeld is directed to a method and apparatus for implementing selected functionality on an integrated circuit device. From a review of the Schoenfeld reference, Applicant respectfully submits that the limitations of existing claims 29 and 35 do not read upon Figures 6a and 6b of Schoenfeld. However, in an effort to expedite prosecution, Applicant has even further clarified the distinction of claims 29 and 35 over the Schoenfeld reference, by amending the claims to clarify that the second portion of the second bond pad of claim 29 for example, is to receive an I/O bond wire for electrically connecting two leads of a package, **"wherein the leads are spaced from periphery of the semiconductor die"**. Somewhat similarly, claim 35 has been amended to clarify that the leads of the package "are spaced from periphery of the semiconductor die". At least such limitations are not taught or suggested by Schoenfeld.

As shown in Figures 6a and 6b of Schoenfeld, for example, even assuming *arguendo* that wire 32 were an I/O bond wire for electrically connecting to a package (which Applicant does not admit), wire 32 is clearly not for connecting to leads of a package, wherein the leads are spaced from the periphery of the semiconductor die, as is now claimed in each of claims 29 and 35 of the present application. The leads 40 as shown in the Schoenfeld reference are lead fingers of a lead frame and thus are internal connections of the device. Further, **the lead fingers are**

spaced over the semiconductor die as shown in Figures 6a and 6b of Schoenfeld, and are not spaced from periphery of the semiconductor die, as is now claimed in each of claims 29 and 35 of the present application. Accordingly, for at least such reasons, withdrawal of the Examiner's rejection of claims 29 and 35, and all claims dependent thereon, is respectfully requested.

Prior Art Rejections under 35 U.S.C. 103

The Examiner has rejected claims 1-2, 6-10, 14-16, 26, and 29-35 under 35 U.S.C. 103 as being unpatentable over Takiar et al. This rejection is respectfully traversed.

Takiar et al. is directed to a stacked multi-chip module and a method of manufacturing thereof. As shown in Figures 5 and 6 of Takiar et al., the multi-chip device includes **a plurality of semiconductor dies 146, 148, and 150** as shown in Figures 5 and 6, and not a single die. Each of the three dies contain bond pads with single lead wires and, as can be seen from Figures 5 and 6, **each of the bond pads is located at a periphery or non-internal portion of each semiconductor die. There are no bond pads located on an internal portion of the semiconductor die.**

Thus, with respect to independent claim 1 for example, there is no teaching or suggestion in Takiar et al. of "a first bond pad...located in an internal portion of the semiconductor die." Somewhat similarly, with regard to claim 9, there is no teaching or suggestion in Takiar et al. of at least "a first electrical termination means....located in an internal portion of the semiconductor die." Accordingly, withdrawal of the Examiner's rejection is respectfully requested.

Additional Prior Art Rejections

Finally, the Examiner rejects dependent claims 3-4, 11-12, and 36-37 under 35 U.S.C. 103 as being unpatentable over Takiar et al. in view of Schoenfeld; rejects claims 5, 13, and 38 as being unpatentable over the alleged combination of Takiar et al. in view of Manning et al.;

and further rejects claim 32 as being unpatentable over the alleged combination of Schoenfled in view of Manning et al. These rejections are respectfully traversed.

Applicant respectfully submits that evening assuming *arguendo* that the secondary references could be combined with the primary references, which Applicant does not admit, Applicant respectfully suggests that each of the aforementioned secondary references would fail to make up for at least the aforementioned deficiencies of the primary references. Accordingly, for at least the reasons previously provided with regard to the corresponding independent claims 1, 9, 29, and 35, Applicant respectfully submits that each of the dependent claims is allowable over the prior art of record, taking singularly or in combination. Accordingly, for at least such reasons previously provided, Applicant respectfully requests withdrawal of each of the Examiner's outstanding rejections.

Entry of this Amendment After Final

Applicant respectfully requests entry of the present Amendment After Final in that the amendments to the claims do not raise any new issues which would require further consideration and/or search. The claim amendments have merely been made to clarify the claims, or to correct minor informalities in the claims, and thus do not raise any new issues which would require any further consideration and/or search. Further, the claim amendments clearly place the claims in an allowable form and thus expedite prosecution of the present application. Accordingly, entry of the present Amendment After Final is respectfully requested.

Still further, as the Examiner's rejection should not have been made final in connection with the present application, Applicant respectfully requests entry of all amendments submitted herewith as a matter of right.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of all outstanding objections and rejections and allowance of each of claims 1-16 and 25-40 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Donald J. Daley, Reg. No. 34,313 at the telephone number (703) 390-3030.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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DJD/bof

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